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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,660	08/22/2003	Eyal Fayneh	INTEL-031	8422

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,660	FAYNEH ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 4, 5, 7, 8, 9, 19, 20, 21, 24, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kizer et al. (US 6,967,514 B2).

Kizer et al. anticipate claim 1.

Kizer et al. teach a system for correcting duty-cycle distortion, comprising: a measurement unit to measure duty-cycle distortion in a clock signal; and a correction unit to dynamically adjust the clock signal to reduce the duty-cycle distortion (col. 3, lines 14-26, lines 34-37, Kizer et al.).

- Kizer et al. anticipate claim 3.

Kizer et al. teach the system, wherein the measurement unit includes: a single-input charge pump driven by the clock signal (fig. 10, col. 2, lines 1-5, col. 3, lines 15-16, lines 46-49, col. 4, lines 12-13, col. 12, lines 12-14, Kizer et al.); and a loop filter to integrate an output of the charge pump to form an analog correction signal for the correction unit (fig. 1A, 1B, 5A, col. 3, lines 51-53, col. 5, lines 28-29, lines 50-51, col. 8, lines 4-6, lines 36-39, Kizer et al.).

- Kizer et al. anticipate claim 4.

Kizer et al. teach the system, wherein the measurement unit computes an average of the output current of the charge pump over a predetermined time, said average output current being proportional to the duty-cycle distortion (fig. 15A, 15B, col. 3, lines 46-49, col. 16, lines 22-63, Kizer et al.).

- Kizer et al. anticipate claim 5.

Kizer et al. teach the system, wherein the measurement unit generates an analog control signal to adjust a duty cycle of the clock signal (col. 3, lines 34-53, col. 5, lines 50-51, Kizer et al.).

- Kizer et al. anticipate claim 7.

Kizer et al. teach the system, wherein the correction unit includes: a delay unit to delay an input signal based on the analog control signal, said delayed input signal corresponding to the frequency signal having reduced duty-cycle distortion (fig. 4B, 4E, col. 6, line 44 to col. 7, line 12, Kizer et al.).

- Kizer et al. anticipate claim 8.

Kizer et al. teach the system, wherein the measurement unit includes a signal generator which generates the analog control signal, said signal generator including: a control unit; a positive current source; and a negative current source, wherein the control unit selectively connects the positive current source and the negative current source to an output node of the signal generator to generate the analog control signal (fig. 15A, 15B, col. 3, lines 46-49, col. 16, lines 22-63, Kizer et al.).

- Kizer et al. anticipate claim 9.

Kizer et al. teach the system, wherein the control unit connects the positive current source and the negative current source to the output node for different periods of time to generate the analog control signal (col. 17, lines 9-41, Kizer et al.).

- Kizer et al. anticipate claim 19.

Kizer et al. teach a method for correcting duty-cycle distortion, comprising: measuring duty-cycle distortion in a clock signal; and dynamically adjusting the clock signal to reduce the duty-cycle distortion (col. 3, lines 14-26, lines 34-37, Kizer et al.).

- Kizer et al. anticipate claim 20.

Kizer et al. teach the method, wherein measuring the duty-cycle distortion includes: measuring durations of high-phase and low-phase portions of the clock signal (fig. 4A, 4B, col. 6, line 44-col. 7, line 12, Kizer et al.).

- Kizer et al. anticipate claim 21.

Kizer et al. teach the method, further comprising: generating an analog control signal based on said durations, wherein the clock signal is adjusted to cause the duration of the high-phase portion of the clock

signal to equal the low-phase portion of the clock signal (col. 3, lines 34-53, col. 5, lines 50-51, Kizer et al.).

- Kizer et al. anticipate claim 24.

Kizer et al. teach a processing system, comprising: a circuit; and a correction unit to correct duty cycle distortion of a frequency signal input into the circuit, said correction unit comprising a measurement unit to measure duty-cycle distortion in a clock signal and a correction unit to dynamically adjust the clock signal to reduce the duty-cycle distortion (col. 1, lines 28-54, col. 3, lines 14-26, lines 34-37, Kizer et al.).

- Kizer et al. anticipate claim 25.

Kizer et al. teach the processing system, wherein said circuit includes a chipset, processor, or memory (col. 1, lines 28-54, Kizer et al.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2, 6, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizer et al. (US 6,967,514 B2) as applied to claim 1 above, and further in view of Davis et al. (US 6,981,185 B1).

As per claim 2, Kizer et al. substantially teach the claimed invention described in claim 1 (as rejected above). Kizer et al. also teach the system, wherein the correction unit adjusts durations of high- phase

and low-phase portions of the clock signal to reduce the duty-cycle distortion (fig. 4A, 4B, col. 6, line 44-col. 7, line 12, Kizer et al.).

However Kizer et al. do not explicitly teach the specific use of reducing the duty-cycle distortion to substantially zero.

Davis et al. in an analogous art teach a bias driver configured to drive the duty cycle error to zero (col. 11, lines 45-46, Davis et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kizer et al.'s patent with the teachings of Davis et al. by including an additional step of reducing the duty-cycle distortion to substantially zero.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that reducing the duty-cycle distortion to substantially zero would provide the opportunity to optimize data transmission in a computer system.

- As per claim 6, Kizer et al. and Davis et al. teach the additional limitations.

Kizer et al. teach the system, wherein the analog control signal adjusts the duty cycle of the clock signal (col. 3, lines 34-37, lines 51-53, col. 5, lines 50-51, Kizer et al.).

Davis et al. teach correcting substantially all the duty-cycle distortion (col. 11, lines 45-46, Davis et al.).

- As per claim 22, Kizer et al. and Davis et al. teach the additional limitations.

Kizer et al. teach the method, wherein the analog control signal adjusts the duty cycle of the frequency signal (col. 3, lines 34-37, lines 51-53, col. 5, lines 50-51, Kizer et al.).

Davis et al. teach correcting substantially all the duty-cycle distortion (col. 11, lines 45-46, Davis et al.).

- As per claim 23, Kizer et al. and Davis et al. teach the additional limitations.

Kizer et al. teach the method, further comprising: delaying an input signal based on the analog control signal, said delayed input signal corresponding to the frequency signal having reduced duty-cycle distortion (fig. 4B, 4E, col. 6, line 44 to col. 7, line 12, Kizer et al.).

6. Claims 10, 11, 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizer et al. (US 6,967,514 B2) in view of Lu (US 6,100,735) and Maneatis (US 5,727,037).

As per claim 10, Kizer et al. teach a duty-cycle correction circuit comprising: a single-input charge pump to receive a core clock signal (fig. 1A, 1B, col. 3, lines 14-16, lines 46-49, Kizer et al.).

However Kizer et al. do not explicitly teach the specific use of a voltage-controlled buffer to generate an output clock signal based on an input clock signal and a control voltage; and a bias generator to generate said control voltage based on an output of the single-input charge pump.

Lu in an analogous art teaches that fig. 1...one period of ICLK (fig. 1, col. 1, lines 36-65, Lu).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kizer et al.'s patent with the teachings of Lu by including an additional step of using of a voltage-controlled buffer to generate an output clock signal based on an input clock signal and a control voltage; and a bias generator to generate said control voltage based on an output of the single-input charge pump.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to change the delay through the voltage controlled buffer to adjust the output clock signal.

Kizer et al. also do not explicitly teach specifically to feedback said control voltage to the single-input charge pump and a single-input charge pump to receive a bias voltage.

Maneatis in an analogous art teach that the DLL 601 also performs duty cycle correction to 50% (fig. 6A, col. 14, lines 59-60, Maneatis). Maneatis also teaches that a bias generator coupled to the loop filter for generating a buffered version of the control voltage and for generating a bias signal that is fed back to the charge pump (col. 15, lines 46-49, Maneatis).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kizer et al.'s patent with the teachings of Maneatis by including an additional step of using the control voltage feedback to the single-input charge pump and a single-input charge pump to receive a bias voltage.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to cause the charge pump to output substantially zero current when the duty cycle of the clock signal is at 50%.

- As per claim 11, Kizer et al., Lu and Maneatis teach the additional limitations.

Lu teaches the circuit, wherein the voltage-controlled buffer corrects the input clock signal to have reduced phase distortion (col. 1, line 61 to col. 2, line 2, Lu).

- As per claim 17, Kizer et al., Lu and Maneatis teach the additional limitations.

Kizer et al. teach the circuit, wherein the single-input charge pump measures duty- cycle distortion of the core clock signal and generates an average current signal proportional to the duty cycle distortion of the core clock signal (fig. 15A, 15B, col. 3, lines 46-49, col. 16, lines 22-63, Kizer et al.).

- As per claim 18, Kizer et al., Lu and Maneatis teach the additional limitations.

Maneatis teaches the circuit, wherein the current signal is converted to a correction voltage, and wherein the correction voltage determines a value of the control voltage (fig. 1, col. 7, lines 2-4, Maneatis).

7. Claims 12, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizer et al. (US 6,967,514 B2), Lu (US 6,100,735) and Maneatis (US 5,727,037) as applied to claim 10 above, and further in view of Ishikawa et al. (US 5,991,221).

As per claim 12, Kizer et al., Lu and Maneatis substantially teach the claimed invention described in claim 10 (as rejected above). Maneatis also teaches a loop filter to provide a correction voltage to the bias generator (fig. 1, col. 7, lines 7-8, Maneatis).

However Kizer et al., Lu and Maneatis do not explicitly teach the specific use of a startup circuit to generate an initial DC bias voltage for the single-input CP.

Ishikawa et al. in an analogous art teach that the power supply circuit...clamped voltage Vfix (fig. 1, col. 10, lines 1-15, Ishikawa et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kizer et al.'s patent with the teachings of Ishikawa et al. by including an additional step of using a startup circuit to generate an initial DC bias voltage for the single-input CP.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a startup circuit to

generate an initial DC bias voltage for the single-input CP would provide the opportunity to cause the charge pump to output current when there is a phase difference.

- As per claim 13, Kizer et al., Lu and Maneatis and Ishikawa et al. teach the additional limitations. Maneatis teaches the circuit, wherein the loop filter converts an output current of the single-input charge pump to the correction voltage (fig. 1, col. 7, lines 2-4, Maneatis).

- As per claim 14, Kizer et al., Lu and Maneatis and Ishikawa et al. teach the additional limitations. Maneatis teaches the circuit, wherein the bias generator compensates for changes in a supply voltage (col. 8, lines 50-54, Maneatis).

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kizer et al. (US 6,967,514 B2), Lu (US 6,100,735) and Maneatis (US 5,727,037) as applied to claim 11 above, and further in view of Van der Veer et al. (US 6,924,480 B2).

As per claim 15, Kizer et al., Lu and Maneatis substantially teach the claimed invention described in claim 10 (as rejected above).

However Kizer et al., Lu and Maneatis do not explicitly teach the specific use of the circuit, wherein a response time is approximately 50 nS.

Van der Veer et al. in an analogous art teach that it may not be necessary to pulse or vary the duty cycle of the voltage supplied to electrode 28 to control heating (col. 5, lines 48-50, Van der Veer et al.). Van der Veer et al. teach ring free networks with a response time of 50 ns (col. 7, lines 58-59, Van der Veer et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kizer et al.'s patent with the teachings of Van der Veer et al. by including an additional step of using the circuit, wherein a response time is approximately 50 nS.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit, wherein a response time is approximately 50 nS would provide the opportunity to optimize data transmission in a computer system.

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kizer et al. (US 6,967,514 B2), Lu (US 6,100,735) and Maneatis (US 5,727,037) as applied to claim 10 above, and further in view of Schultz et al. (US 6,191,613 B1).

As per claim 16, Kizer et al., Lu and Maneatis substantially teach the claimed invention described in claim 10 (as rejected above).

However Kizer et al., Lu and Maneatis do not explicitly teach the specific use of the circuit, further comprising: a global clock network to distribute the output clock signal.

Schultz et al. in an analogous art teach that global clock network 235 is a buffered clock tree that distributes the data-clock signal (fig. 2, col. 3, lines 24-25, Schultz et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kizer et al.'s patent with the teachings of Schultz et al. by including an additional step of using the circuit, further comprising: a global clock network to distribute the output clock signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit, further comprising: a global clock network to distribute the output clock signal would provide the opportunity to distribute the clock signal to different system components.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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